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EXAMINER	
RADOSEVICH, STEVEN D	

ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/528,328	KAY, ANDREW	
	Examiner	Art Unit	
	STEVEN D. RADOSEVICH	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 March 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/18/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-31 are present within this initial examination.

Priority

Acknowledgment is made that foreign Priority is claimed for this application to United Kingdom application 02218683 (in English) with the date 9/20/2002, therefore this initial examination will be using the 9/20/2002 date for the purposes of this examination.

Information Disclosure Statement

Acknowledgment is made that an Information Discloser Statement (IDS) was filed prior to this initial examination and therefore has been reviewed and contents disclosed considered. Examiner notes the IDS discloses one (1) U.S. Patent Document, four (4) Foreign Patent Documents, and one (1) Other Art Document.

Claim Objections

Claims 1, 11, and 13 are objected to because of the following informalities:

Claim 1: A typographical error exists wherein the word "charactorised" within the claims preamble should be replaced with "characterized" as is believed what was intended.

Claims 11 and 13: same typographical error as in claim 1 within the body of the claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 14-16 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Examiner notes that the claims are drawn to a computer program and therefore are non-statutory under 35 U.S.C. 101 since a computer program is an abstract idea and does not require a physical transformation, and the claimed invention does not produce a useful, concrete, and tangible result. Therefore claims 14-16 will not be given any further consideration within this examination since that which is claims in non-statutory.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-16, 17-30, and 31 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claims 1, 17, and 31, the claim is unclear to the examiner since the claim does not reflect to one of ordinary skill within the art the invention in view of the discloser describing the invention (see the specification pages 6 lines 8-18 and page 11 lines 6-7). Specifically it is unclear when the action is performed if ever since any determined pointer points to an address within the range of the memory block including the last new memory location (i.e. 4 will always be within the range of 0-5).

Claims 2-16 and 18-30 are dependent upon claims 1 and 17 respectfully and therefore also inherits the 35 U.S.C. 112, second paragraphs issues of their respective independent claim and may not be further considered on their merits.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-6, 8, 11-13, 17-22, 24, and 27-31 are rejected under 35 U.S.C. 102(b) as being anticipated by Teich et al (U.S. Publication 20010007108 A1, filed 12/22/2000 and published 7/5/2001).

1. As per claims 1, 17, and 31, Teich teaches a method of detecting an error in a persistent memory segment in which values of at least one data item are stored in temporally consecutively allocated locations, each new memory location is added to a first end of a block of the memory segment having first and second ends, and a pointer to each new memory location is added to an older memory location in the block containing a preceding value of the at least one data item (Linked list and EEPROM: paragraph 0049, abstract, and figures 3A-B), the method being characterized by comprising:

a. determining the address to which the last-added pointer points (new (current) record is 'active' in paragraph 0073);

b. comparing the determined address with an address range of the memory block including the last new memory location (LUM) (paragraph 0073 with respect to the previous record is 'fully active' and paragraphs 0062-0063 with 0066-0067) ; and

c. performing an action if the determined address is outside the address range (modify in paragraph 0075).

2. As per claims 2 and 18, Teich teaches wherein the steps (a) to (c) are performed each time power is applied to the memory segment (paragraph 0068.

3. As per claims 3 and 19, wherein the step (a) comprising determining the addresses to which all of the pointers point and selecting the highest or lowest address (new (current) record in paragraph 0073 and last appended (current record in paragraph 0062).

4. As per claims 4 and 20, wherein the step (c) comprises changing the address of the last-added pointer to the address of the last new memory location ('fully active' in paragraph 0075).

5. As per claims 5 and 21, wherein each new memory location is added contiguously to the first end of the block (linked list in paragraph 0069, and 0049, and figures 3A-B).

6. As per claims 6 and 22, wherein each pointer points to a highest or lowest address of the memory location to which it points linked list in paragraph 0069, and 0049, and figures 3A-B).

7. As per claims 8 and 24, wherein each memory location has space for a single value of the at least one data item (data in paragraphs 0009-0010, linked list in paragraphs 0049 and 0069, and figures 3A-B).

8. As per claims 11, 12, 27, and 28, wherein the memory segment contains at least one write counter in which a respective flag is set at the end of each value storing operation and a respective further flag is set at the end of each pointer adding operation, and also characterized in that the steps (a) to (c) are performed only if an odd number of flags and further flags is set ('active' and 'fully active' in paragraphs 0072-0079).

9. As per claims 13 and 29, wherein the memory segment contains at least one write counter in which, when storing a series or one or more data item values, a respective flag is set before the first pointer adding operation in the series and a respective further flag is set after the final pointer adding operation in the series, and also characterized in that the steps (a) to (c) are performed only if an odd number of flags and further flags is set ('active' and 'fully active' in paragraphs 0072-0079).

10. As per claim 30, Teich teaches comprising a smart card (chip cards in paragraph 0003).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 7, 9, 10, 23, 25, and 26, are rejected under 35 U.S.C. 103(a) as being unpatentable over Teich et al (U.S. Publication 20010007108 A1) as applied to claims 1 and 17 respectively above, and further in view of AAPA (Applicants Admitted Prior Art within U.S. Publication 20060143541 A1).

11. As per claims 7 and 23, Teich teaches as described above lined list with power failure and subsequent recovery dealing with EEPROM memory (title, abstract, and paragraph 0011).

Teich does not specifically teach wherein the memory segment comprises at least part of a flash memory.

AAPA teaches within the background art that EEPROM and Flash memory are different variations of RAM (paragraph 0004).

Therefore one of ordinary skill within the art at the time the invention was made could have been motivated to modify Teich so as to replace the EEPROM with Flash memory since as indicate within AAPA they are both types of RAM and thus equally applicable wherein RAM is used.

12. As per claims 9 and 25, Teich teaches as described above lined list with power failure, subsequent recovery dealing with EEPROM memory, and the action is performed when the detected address is greater than the highest address of the address range (paragraph 0075 and figures 3A-B).

Teich does not specifically teach wherein each bit of the memory segment is individually switchable only from 1 to 0.

AAPA teaches memory individually switchable only from 1 to 0 (paragraph 0010).

Therefore one of ordinary skill within the art at the time the invention was made could have been motivated to have the memory within Teich individually switchable only from 1 to 0 as AAPA teaches since a memory must have a base/reset/clear/erased value/state as AAPA teaches (paragraph 0010) and switchable only from 1 to 0 is a well known proven and reliable way to write date onto a memory.

13. As per claims 10 and 26, Teich teaches as described above lined list with power failure, subsequent recovery dealing with EEPROM memory, and the action is performed when the detected address is less than the highest address of the address range (paragraph 0075 and figures 3A-B).

Teich does not specifically teach wherein each bit of the memory segment is individually switchable only from 0 to 1.

AAPA teaches memory individually switchable only from 1 to 0 (paragraph 0010) as noted above.

Therefore one of ordinary skill within the art at the time the invention was made could have been motivated to have the memory within Teich individually switchable only

from 0 to 1 as since a memory must have a base/reset/clear/erased value/state switchable/changeable for writing as AAPA teaches (paragraph 0010), and it would have been obvious to one having ordinary skill within the art at the time the invention was made to inverse the base/reset/clear/erased value/state form 1 as in AAPA to 0 since the examiner takes official notice of the equivalence of the base/reset/clear/erased value/state being a 1 (high) and a 0 (low) for their use in being the base/reset/clear/erased value/state of the memory and the selection of there known equivalents to be the base/reset/clear/erased value/state of the memory would be within the level of ordinary skill. Examiner notes the base/reset/clear/erased value/state within any binary system can only be either a 1 or a 0 as is well known within the art.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

i. IEEE 100 (see attached and 892 references cited) defines linked list and linked linear list.

ii. Harris et al (U.S. Patent 5873097), Seather (U.S. Patent 5469562), and Spiro et al (U.S. Patent 5369757) all disclose linked list along with and error/fault/failure because of power loss.

iii. Hundt et al (U.S. Patent 713115 B2) discloses stack memory equivalent to linked list memory and comparing a value to the address ranges of modules holding values

iv. Wolrich et al (U.S. Patent 7337275 B2) discloses linked list, pointer, queue memory, and inserting new data.

v. Baba (U.S. Publication 20020027508 A1) and Sadhasivan et al (U.S. publication 20020128994 A1) both disclose power failure, and recovery within flash memory.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to STEVEN D. RADOSEVICH whose telephone number is (571)272-2745. The examiner can normally be reached on 9am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques H. Louis can be reached on 571-272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Cynthia Britt/
Primary Examiner, Art Unit 2117

Steven D. Radosevich
Examiner
Art Unit 2117